

2 including:

3 a plurality of the sections defined thereon by
4 scribe lines, each chip section having bump electrodes
5 formed simultaneously thereon, the scribe lines for
6 separating the chip sections from each other without
7 dividing bump electrodes thereon, said chip section
8 including:

9 a plurality of chip electrodes positioned on said
10 chip section; and

11 a plurality of interconnection layers for
12 electrically connecting said chip electrodes and said
13 bump electrodes,

14 said bump electrodes being located at positions
15 other than over said chip electrodes,

16 said chip section having a center and a periphery
17 and said interconnection layers extend from said
18 periphery toward said center.

1 Claim 11 (three times amended). A semiconductor wafer,
2 including:

3 a plurality of chip sections defined thereon by
4 scribe lines, each chip section having:

5 bump electrodes formed simultaneously thereon;

6 a plurality of chip electrodes positioned on said
7 chip section; and

8 a plurality of interconnection layers for
9 electrically connecting said chip electrodes and said
10 bump electrodes,

11 said bump electrodes being located at positions
12 other than over said chip electrodes,

13 said chip section having a center and a periphery
14 and said interconnection layers extend from said
15 periphery toward said center.